TSEK03: Radio Frequency Integrated Circuits (RFIC)

Lecture 7: Passive Devices

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Overview

- Razavi: Chapter 7

  7.1 General considerations

  7.2 Inductors

  7.3 Transformers

  7.4 Transmission lines

  7.5 Varactors

  7.6 Constant capacitors

7.1 General considerations

- Reduction of off-chip components => Reduction of system cost. Integration is good!
- On-chip inductors:

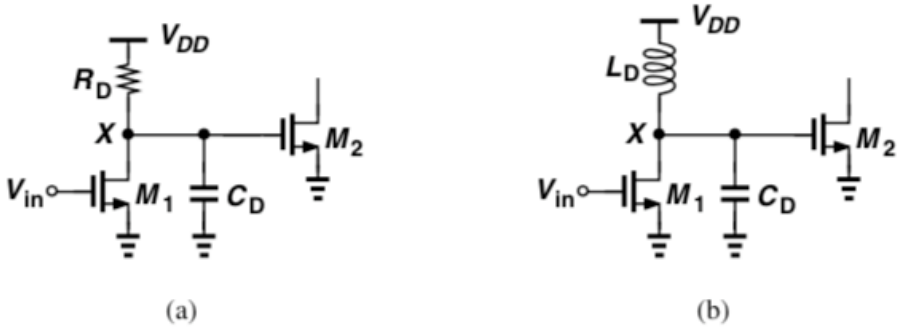
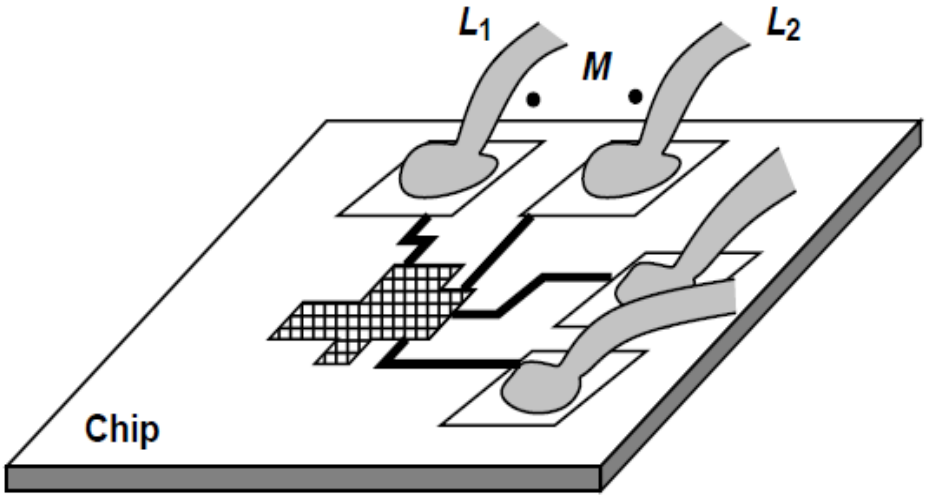


Figure 7.1 *CS stage with (a) resistive, and (b) inductive loads.*

- With inductive loads (b), we can obtain higher operating frequency and better operation at low supply voltages.

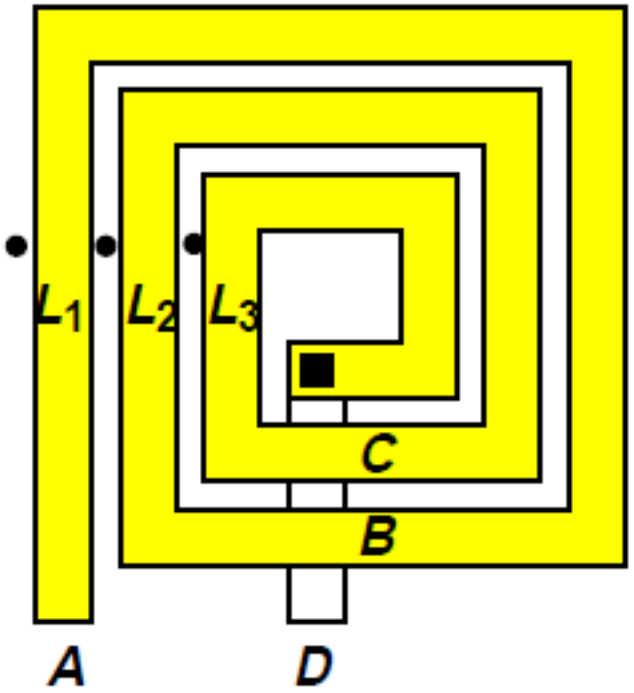
Bond wires = good inductors

- High quality
- Hard to model
- The bond wires and package pins connecting chip to outside world may experience significant coupling, creating crosstalk between parts of a transceiver.



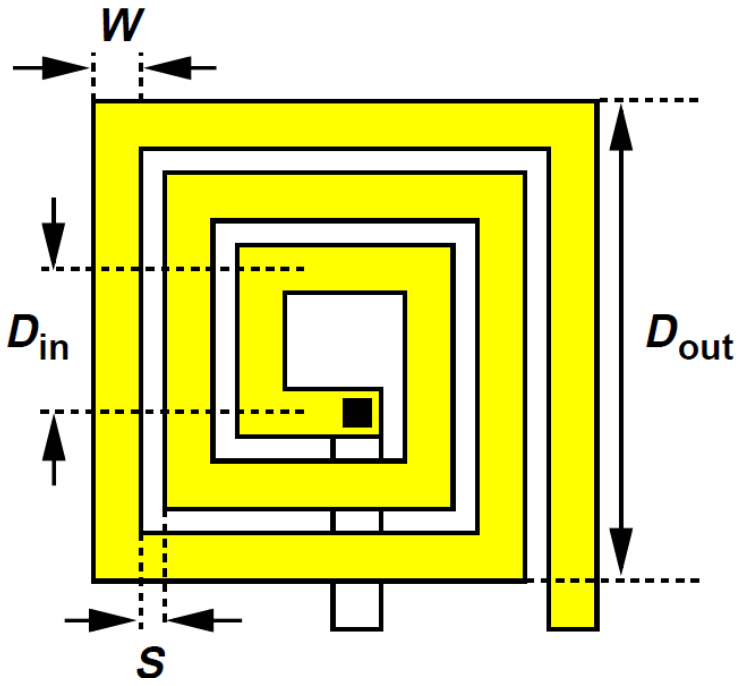
7.2 Inductors

- Typically realized as metal spirals.
- Larger inductance than a straight wire.
- Spiral is implemented on top metal layer to minimize parasitic resistance and capacitance.



$$L_{tot} = L_1 + L_2 + L_3 + M_{12} + M_{13} + M_{23}.$$

- A two dimensional square spiral inductor is fully specified by the following four quantities:
  - Outer dimension, Dout
  - Line width, W
  - Line spacing, S
  - Number of turns, N
- The inductance primarily depends on the number of turns and the diameter of each turn

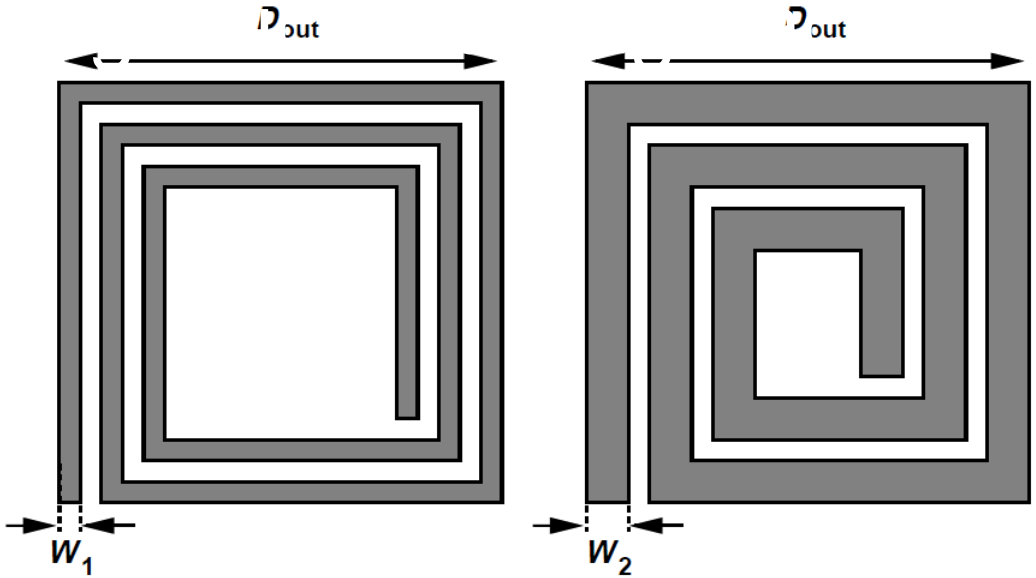


Example 7.3

The line width of a spiral is doubled to reduce its resistance; D_{out}, S, and N remain constant. How does the inductance change?

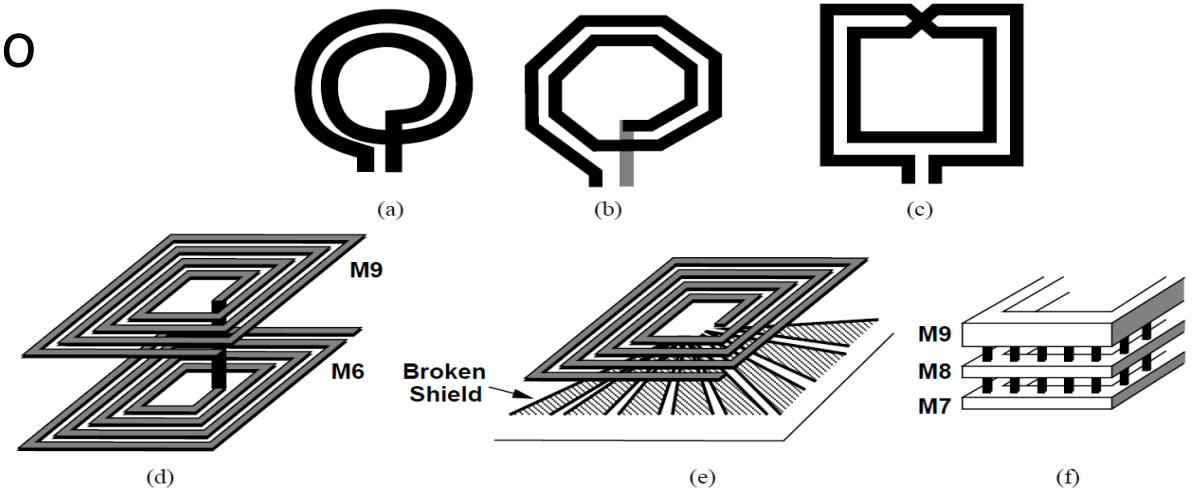
Solution:

As illustrated in Fig. 7.6, the doubling of the width inevitably decreases the diameter of the inner turns, thus lowering their inductance, and the larger spacing between the legs reduces their mutual coupling. We note that further increase in W may also lead to *fewer* turns, reducing the inductance.



Inductor Structures in RFICs

- Various inductor geometries shown below are result of improving the trade-offs in inductor design, specifically those between (a) quality factor and the capacitance, (b) inductance and the dimensions.
- Note: These various inductor geometries provide additional degrees of freedom but also complicate the modeling task.



Inductance calculations

- Closed form inductance equations can be found based on (1) Curve fitting methods, (2) Physical properties of inductors.
- This equation is an empirical formula which estimates inductance of 5 nH to 50 nH square spiral inductor within 10% error:

$$L \approx 1.3 \times 10^{-7} \frac{A_m^{5/3}}{A_{tot}^{1/6} W^{1.75} (W+S)^{0.25}},$$

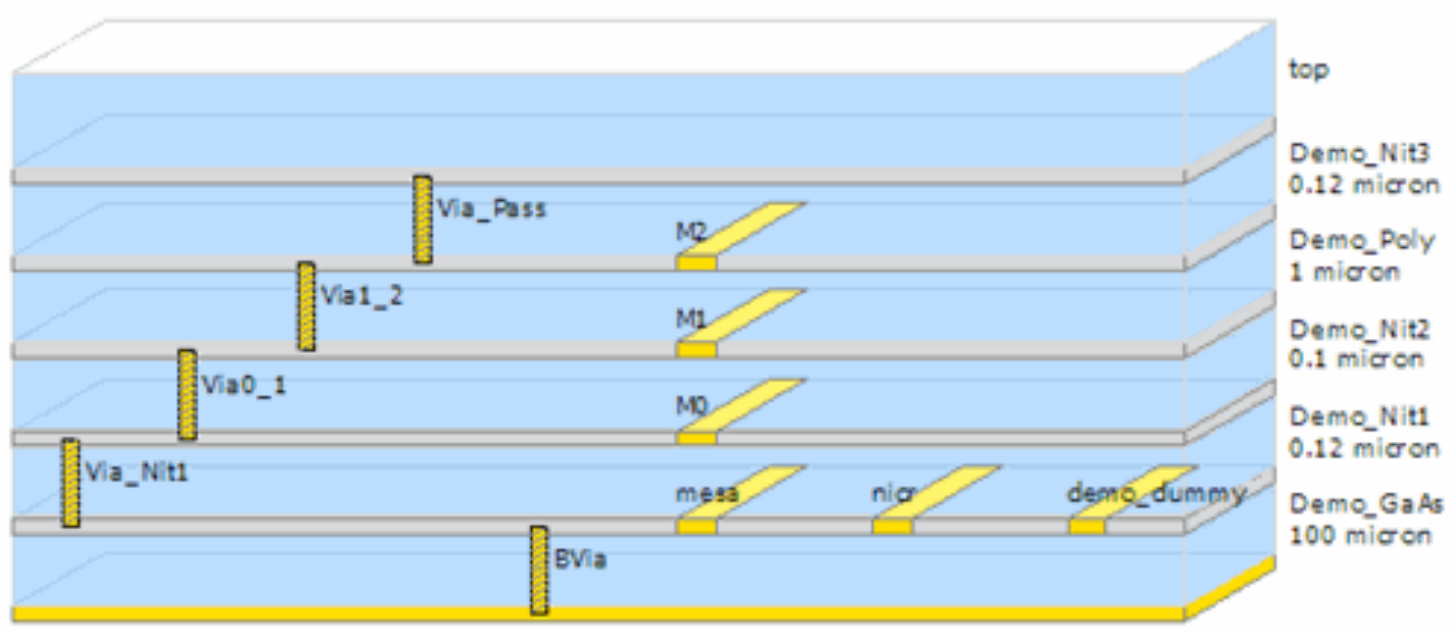
A_m – Metal area , A_{tot} – Total Inductor area

Inductance calculations

- Already modeled inductors in a PDK library may exist
- Otherwise: EM simulations
- Popular tools:
  - Momentum (Keysight), integrated with ADS and Cadence Virtuoso. 2.5 D
  - HFSS (Ansoft): 3D
  - Sonnett
  - (Asitic in the book: old, student work…)
- Output: linear model (n-port s-parameter), frequency range

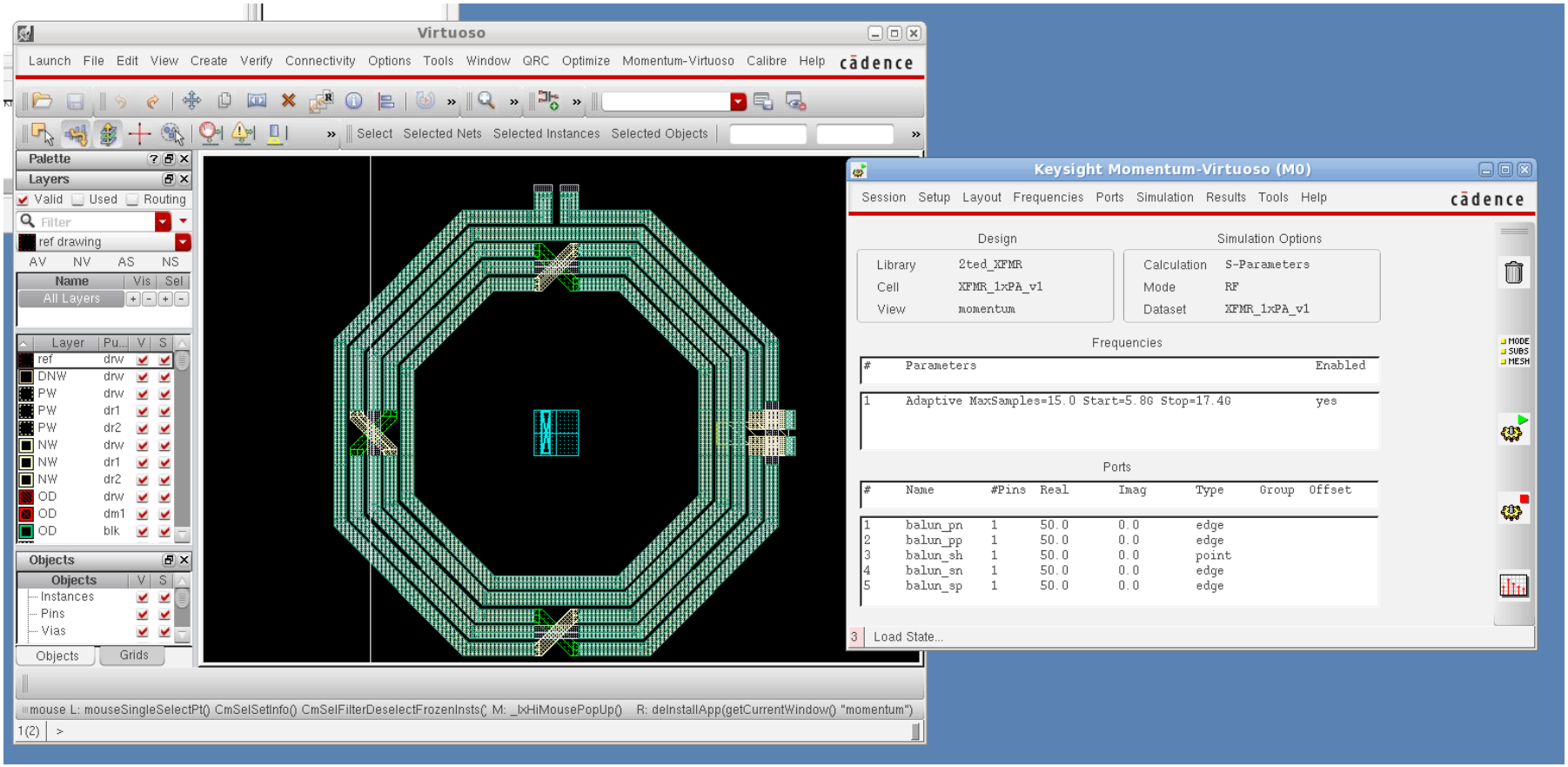
Example: Momentum

- Technology file with layers, vias, resistivities, etc., usually supplied by the PDK vendor.
- Or can be created by a user, if enough information is given in the design manual.



Example: Momentum

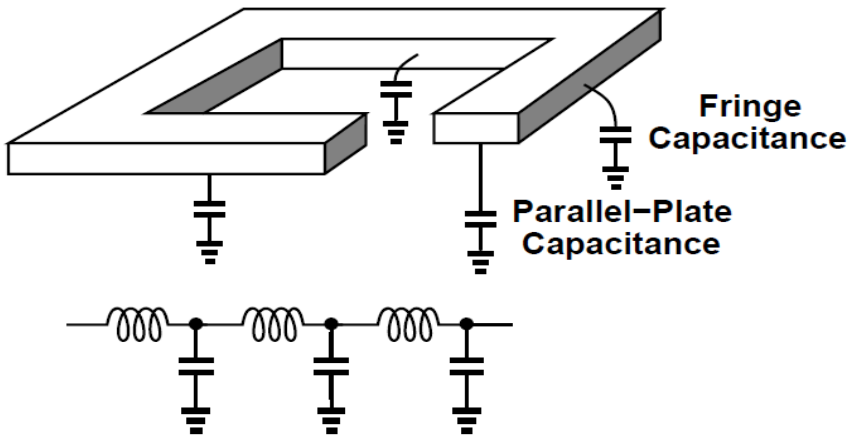
- Cadence integration (example with transformer = double ind)



Parasitic Capacitance of Integrated Inductors

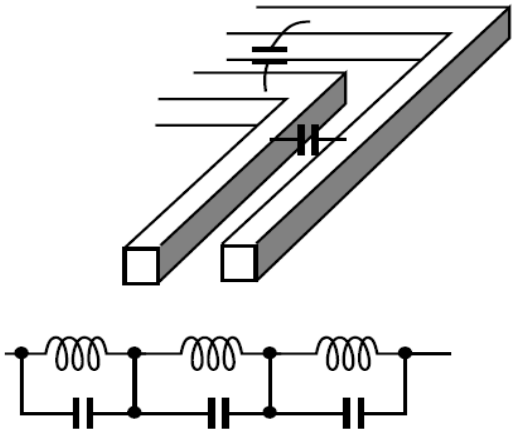
- Planar spiral inductor suffers from parasitic capacitance because the metal lines of the inductor exhibit parallel plate capacitance and adjacent turns bear fringe capacitance.

Bottom-Plate capacitance



(a)

Interwinding capacitances



(b)

Self-resonance frequency

- The frequency at which an inductor resonates with its own capacitances is called the “self-resonance frequency” (f_{SR}).
- The inductor behaves as a capacitor at frequencies above f_{SR}. For this reason, f_{SR} serves as a measure of the maximum frequency at which a given inductor can be used.

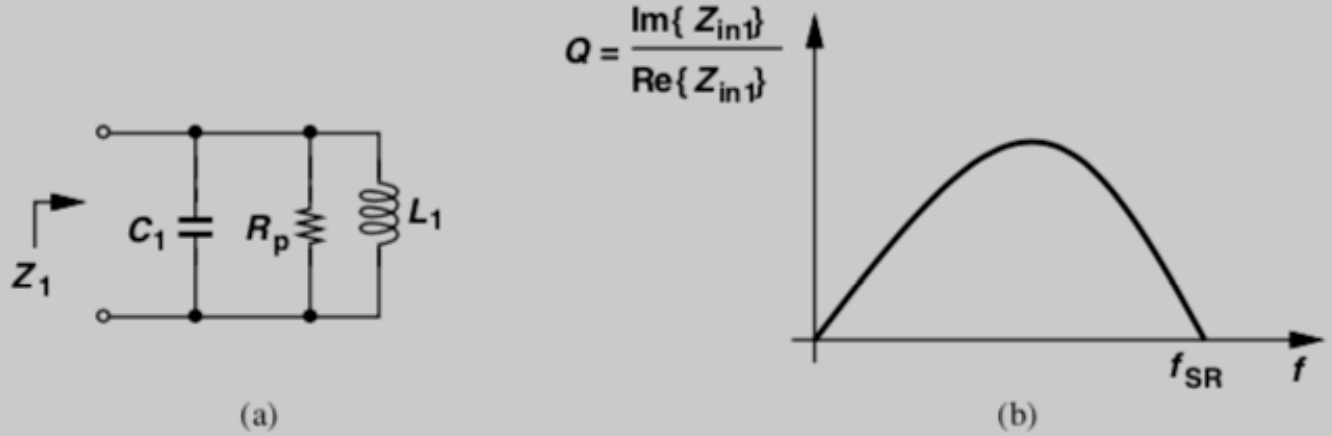
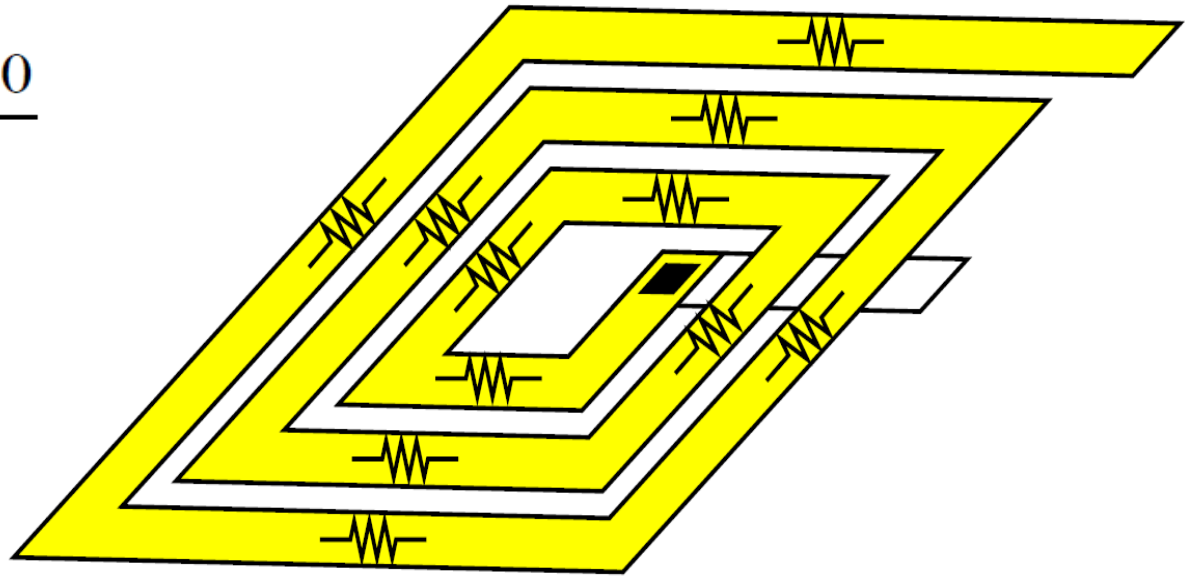


Figure 7.16 *(a) Simple tank and (b) behavior of one definition of Q.*

7.2.5 Loss Mechanisms: Metal Resistance

- Metal resistance R_s of spiral inductor of inductance L_1
- Q = Quality factor of the inductor (measure of loss in the inductor)

$$Q = \frac{L_1 \omega_0}{R_S}$$



Book "For example, a 5-nH inductor operating at 5 GHz with an R_S of 15.7 has a Q of 10."

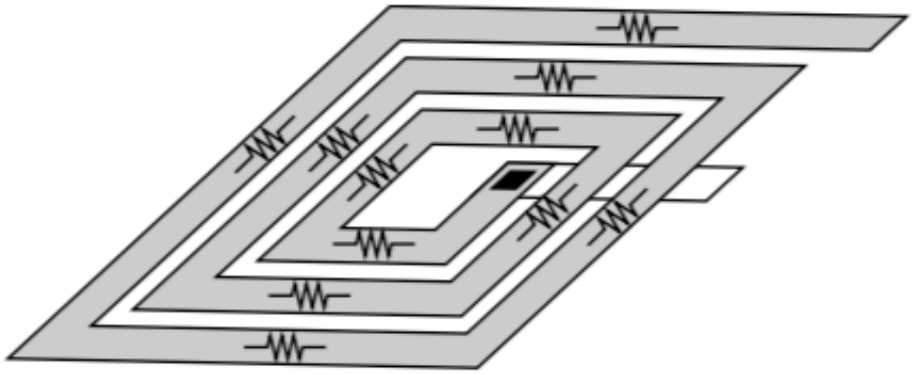
Example 7.9

Assuming a sheet resistance of 22 mΩ/□ for the metal, $W = 4\,\mu m$, and $S = 0.5\,\mu m$, determine if the above set of values is feasible.

Solution:

Recall from our estimates in Section 7.2.3, a 2000-μm long, 4-μm wide wire that is wound into $N = 5$ turns with $S = 0.5\,\mu m$ provides an inductance of about 4.96 nH. Such a wire consists of $2000/4 = 500$ squares and hence has a resistance of $500 \times 22\ m\Omega/\square = 11\ \Omega$. It thus appears that a Q of 10 at 5 GHz is feasible.

$$Q = \frac{L_1 \omega_0}{R_S}$$



Example 7.11

A student reasons that placing m spiral inductors in parallel may in fact *degrade* the Q because it leads to an m-fold decrease in the inductance but not an m-fold decrease in resistance. Explain the flaw in the student's argument.

Solution:

Since the vertical spacing between the spirals is much less than their lateral dimensions, each two experience a strong mutual coupling (Fig. 7.20). If $L_1 = L_2 = L_3 = L$ and $M \approx L$, then the overall inductance remains equal to L (why?).

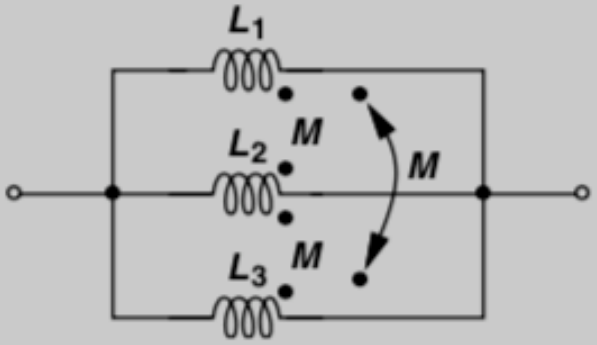
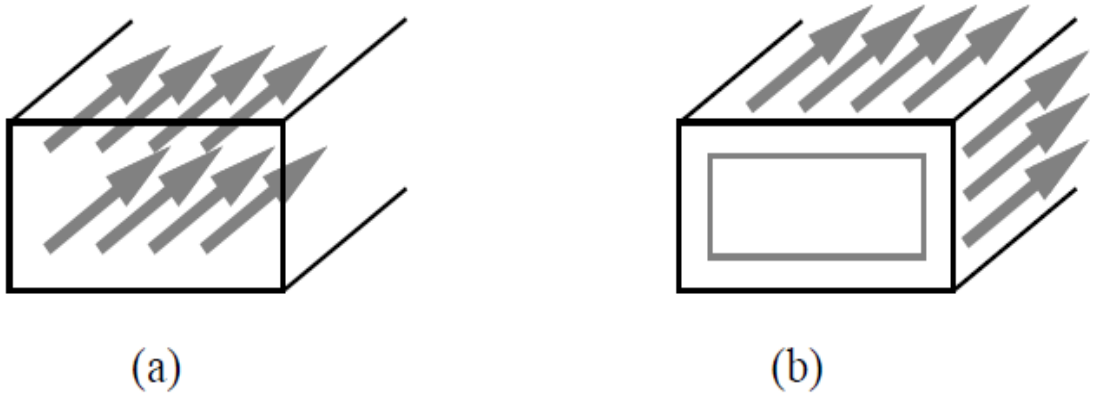


Figure 7.20 *Effect of placing tightly-coupled inductors in parallel.*

Loss Mechanisms: Skin Effect

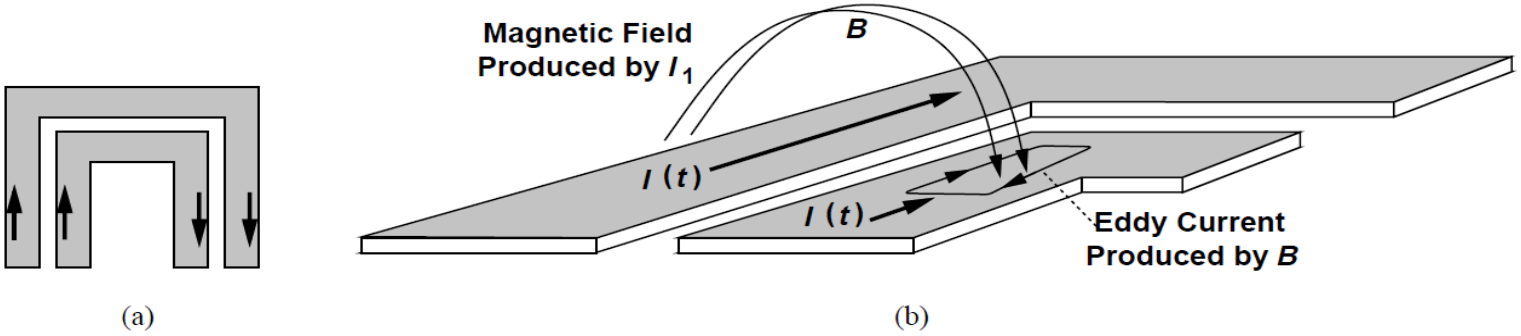
- Current distribution in a conductor at
  (a) Low frequency (b) High frequency



Skin depth = $\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$

Extra resistance = $R_{skin} = \frac{1}{\sigma \delta}$

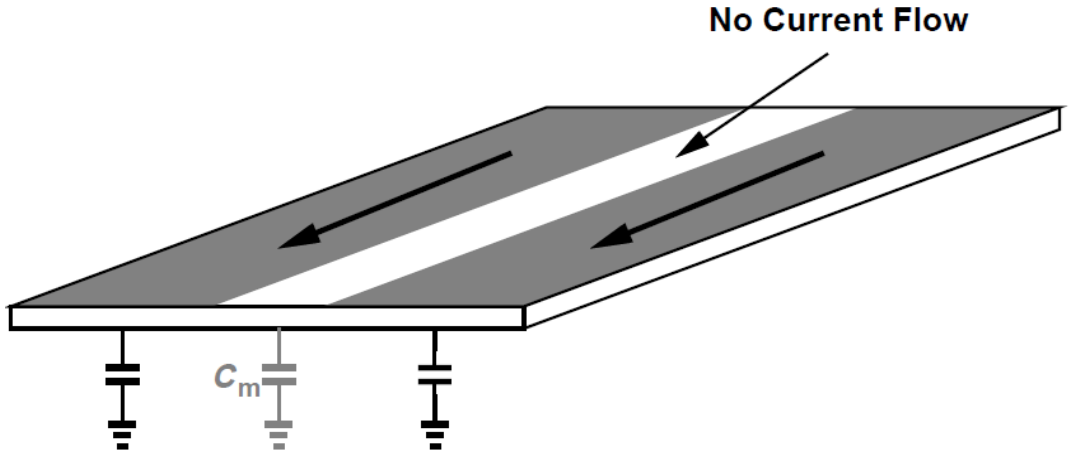
Loss Mechanisms: Current crowding



- At f_{crit} , the magnetic field produced by adjacent turn induces eddy current, causing unequal distribution of current across the conductor width, hence altering the effective resistance of the turn.

$$R_{\text{eff}} \approx R_0 \left[1 + \frac{1}{10} \left(\frac{f}{f_{crit}} \right)^2 \right] \qquad f_{crit} \approx \frac{3.1}{2\pi\mu} \frac{W+S}{W^2} R_{\square}.$$

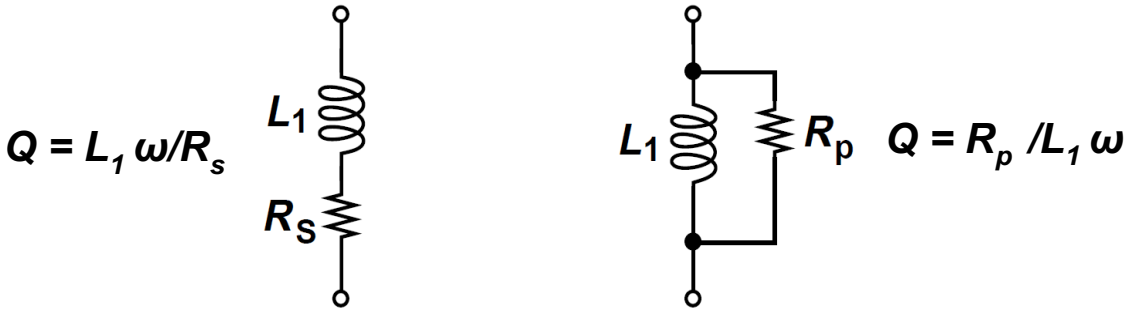
Loss Mechanisms: Current crowding



- As current flows through a smaller width of conductor, this causes a reduction in the effective area between the metal and substrate, hence there is a reduction in the total capacitance.

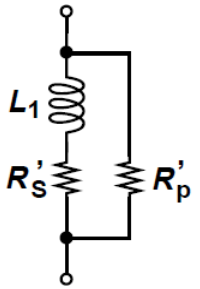
$$C_{tot} \approx \frac{R_0}{R_{\text{eff}}} C_0$$

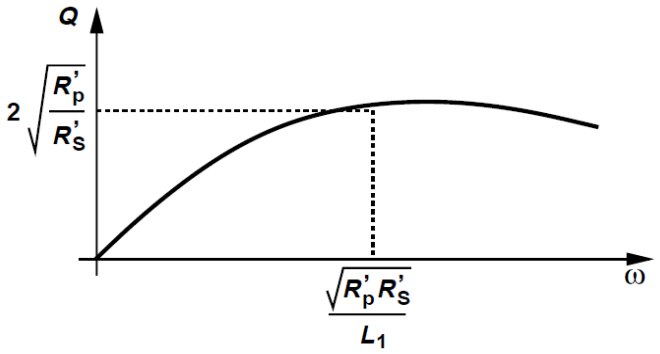
7.2.6 Inductor Modeling



- A constant series resistance R_s model inductor loss for limited range of frequencies.
- A constant parallel resistance R_p model inductor loss for narrow range of frequencies.
- Note: The behavior of Q of inductor predicted by above two models has suggested opposite trends of Q with frequency.

Modeling Loss by Both Series and Parallel Resistors



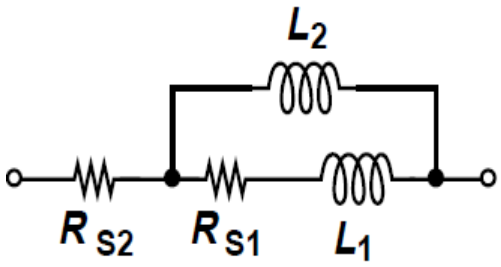


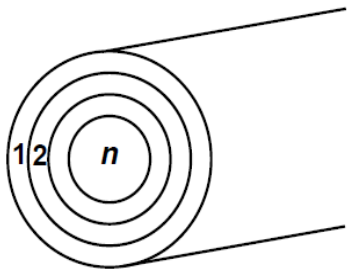
$$R'_S = \frac{L_1\omega}{2Q}$$

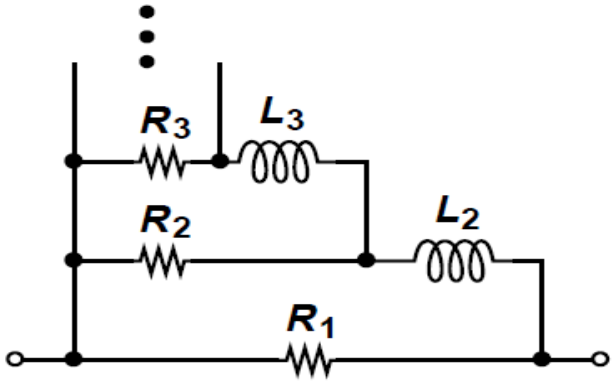
$$R'_p = 2QL_1\omega$$

$$Q = \frac{L_1\omega R'_p}{L_1^2\omega^2 + R'_S(R'_S + R'_p)}$$

Broadband Model of Inductor







Simple model

Model with skin effect

- At low frequencies current is uniformly distributed thorough the conductor and model reduces to $R_1 || R_2 || ..... || R_n$
- As frequency increases the current moves away from the center of the conductor, as modeled by rising impedance of inductors in each branch.

Compact inductor models

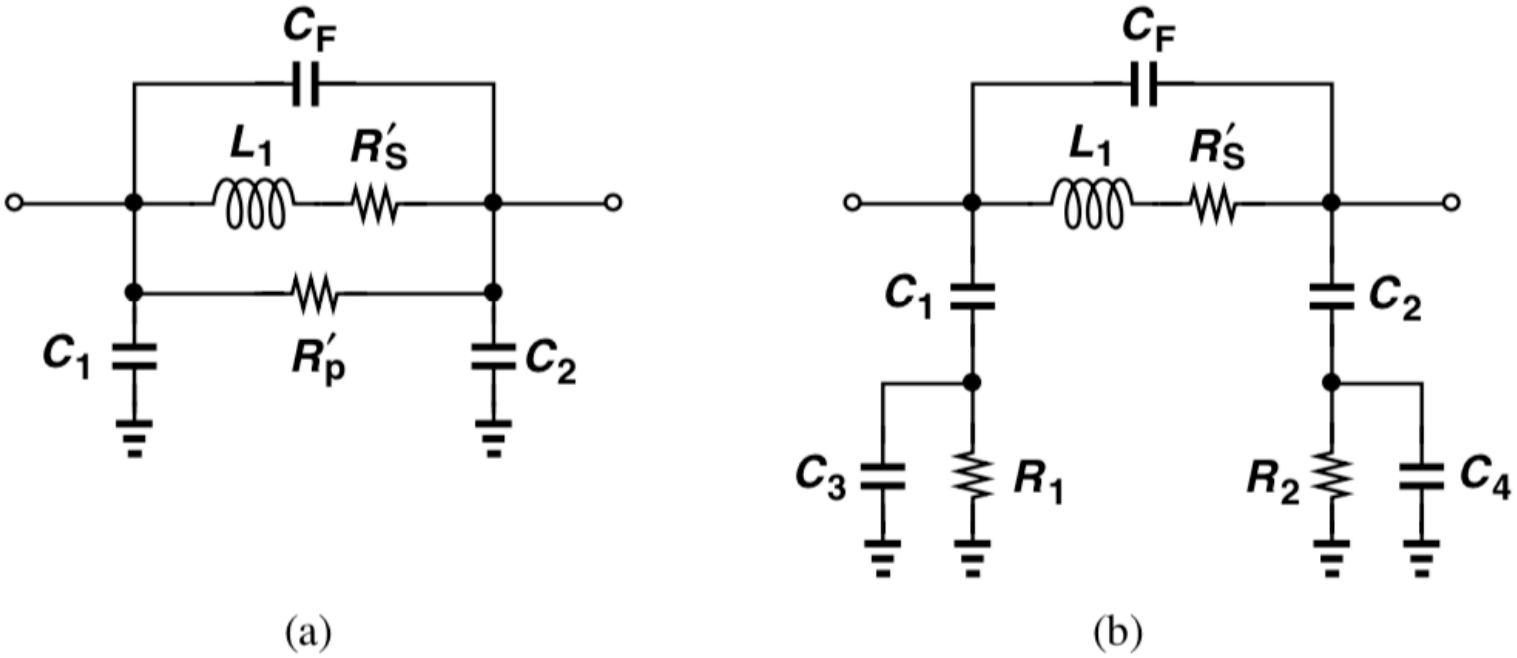
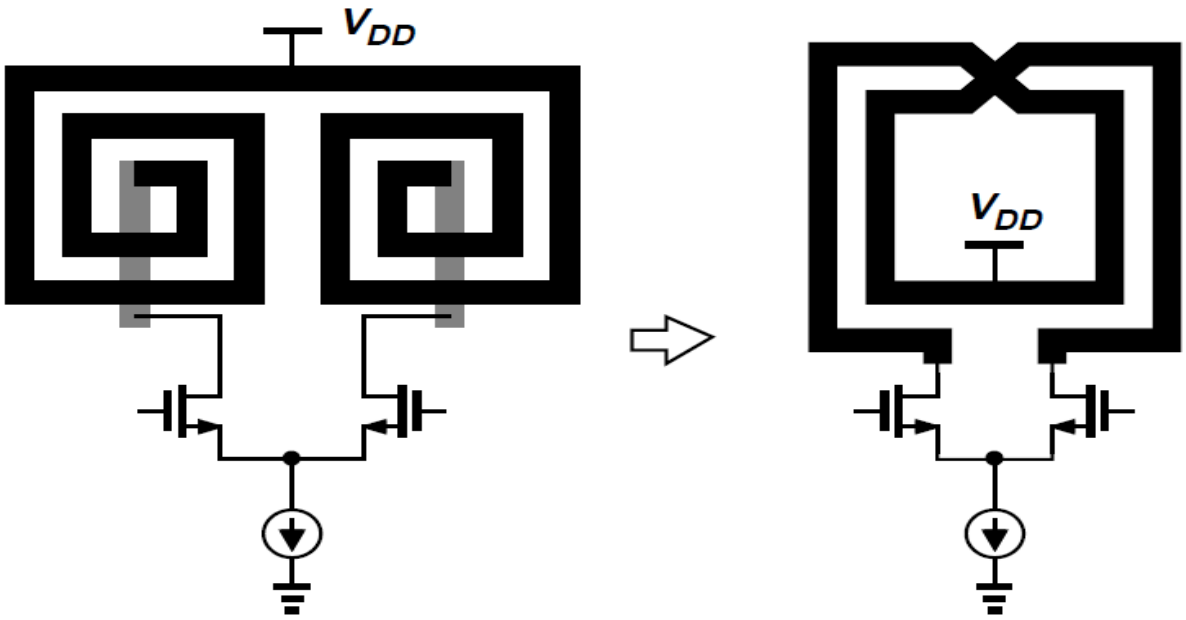


Figure 7.35 *(a) Compact inductor model, (b) alternative topology.*

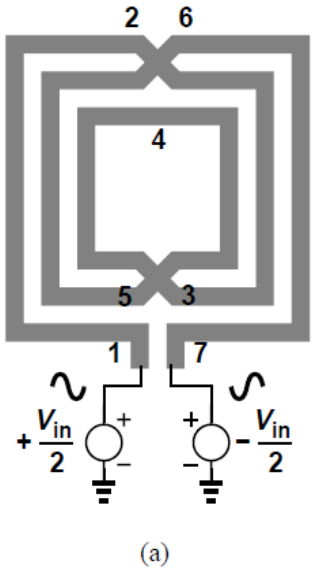
Symmetrical inductor

- Differential circuits can employ a single symmetric inductor instead of two asymmetric inductors. Saves area and have high Q, but higher interwinding capacitance (lower f_{SR}).

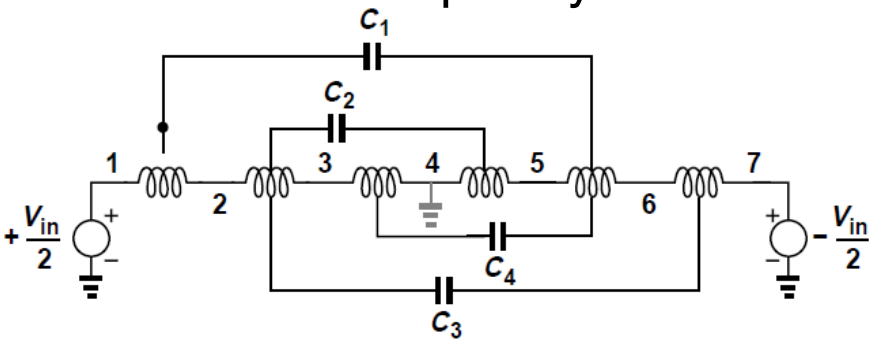


Equivalent Lumped Interwinding Capacitance

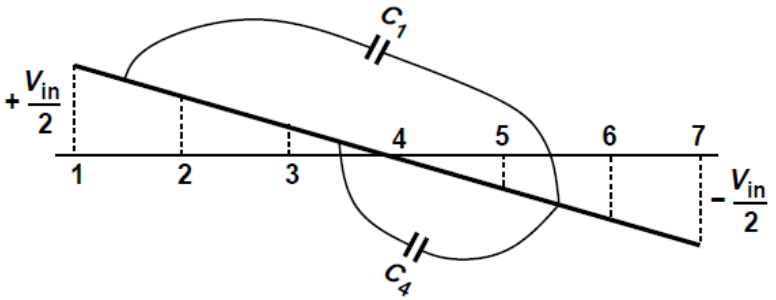
- We unwind the structure as depicted below, assuming that all unit inductances are equal and so are all unit capacitances.
- Resulting equivalent lumped interwinding capacitance of a symmetrical inductor is typically much larger than capacitance of substrate, dominating self resonance frequency.



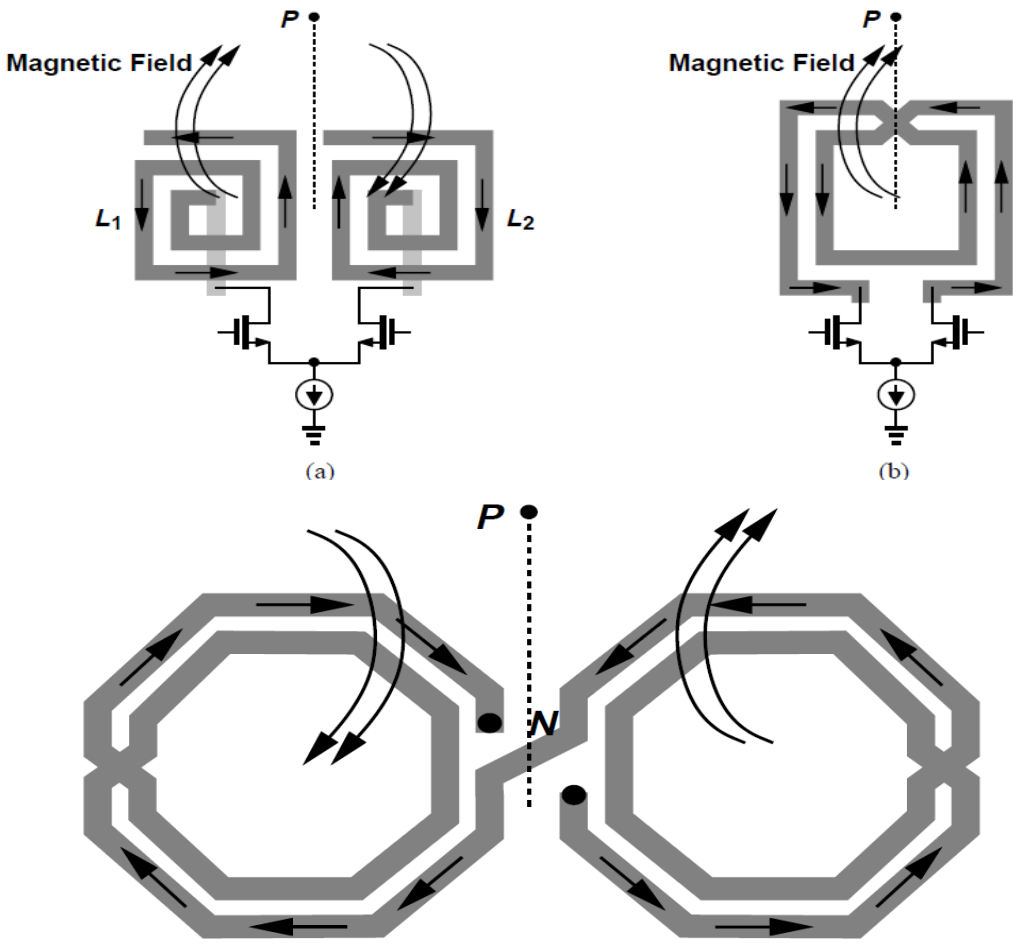
(a)



(b)

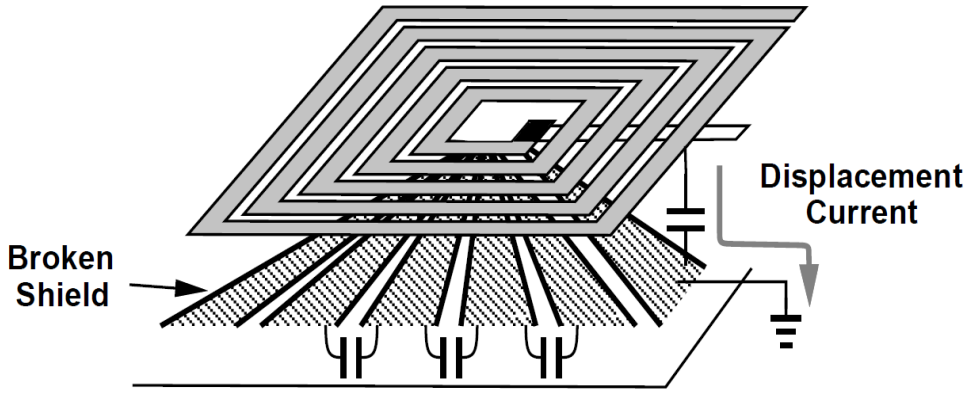


Inductor magnetic coupling



Inductors with Ground Shield

- This structure allows the displacement current to flow through the low resistance path to ground to avoid electrical loss through substrate.
- Eddy currents through a continuous shield drastically reduce inductance and Q, so a “patterned” shield is used.
- This shield reduces the effect of capacitive coupling to substrate.
- Eddy currents of magnetic coupling still flows through substrate.

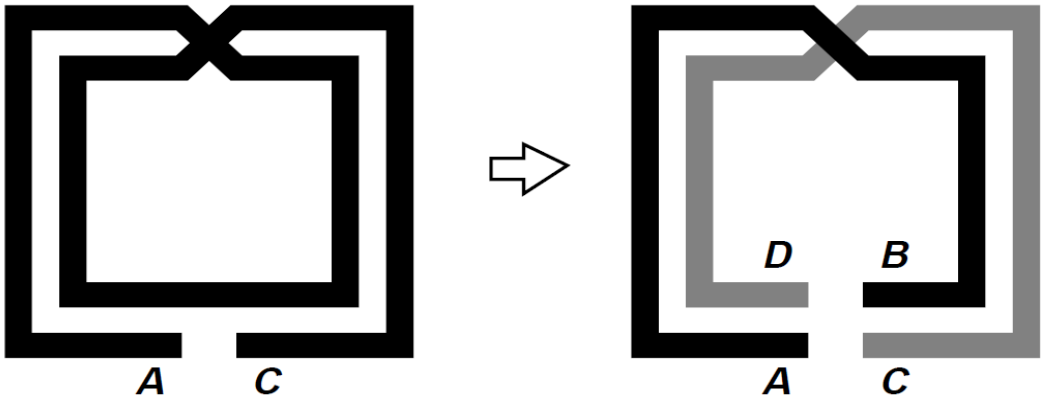


7.3 Transformers

- Useful function of transformer in RF Design:
  - Impedance matching.
  - Feedback and feedforward with positive and negative polarity.
  - Single-ended to differential conversion and vice-verse.
  - AC coupling between stages.
- Well-designed transformer:
  - Low series resistance in primary and secondary windings.
  - High magnetic coupling between primary and secondary windings.
  - Low capacitive coupling between primary and secondary windings.
  - Low parasitic capacitance to the substrate.

Transformer Structures

- Transformer derived from a symmetric inductor:
  - Segments AB and CD are mutually coupled inductors.
  - Primary and secondary are identical so this is a 1:1 transformer



$$L_{AC} = 2L_{AB} + 2M$$

Transformer Structures: examples - I

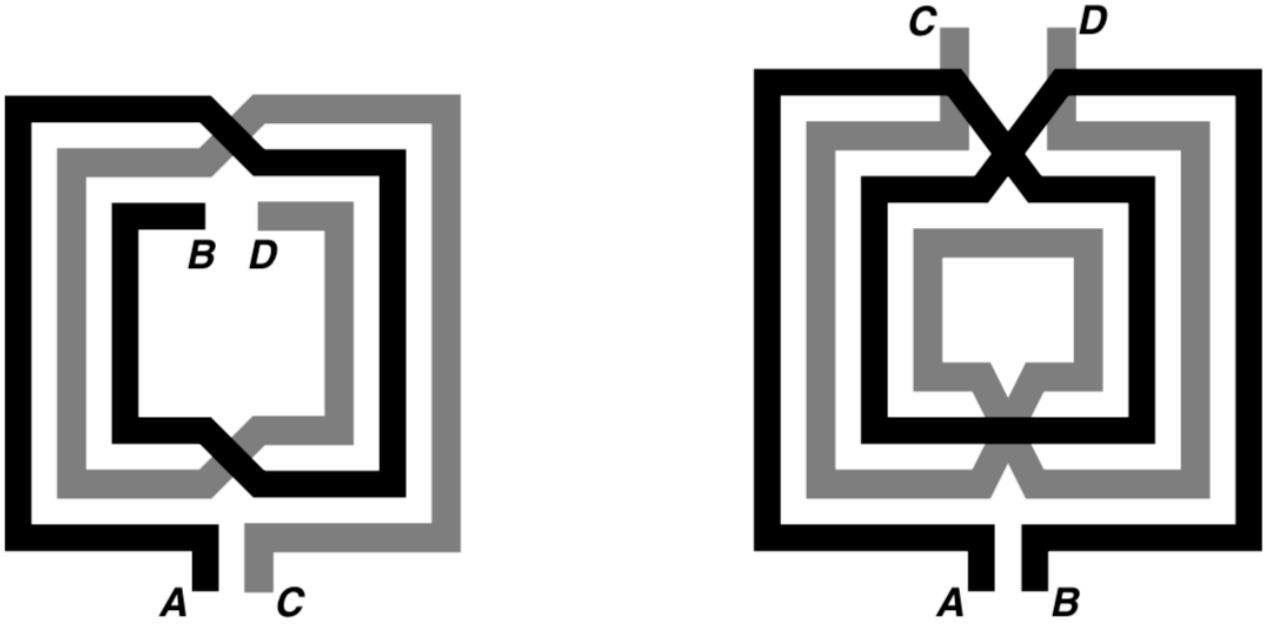


Figure 7.49 *Transformers (a) derived from a three-turn symmetric inductor, (b) formed as two embedded symmetric spirals.*

Transformer Structures: examples - II

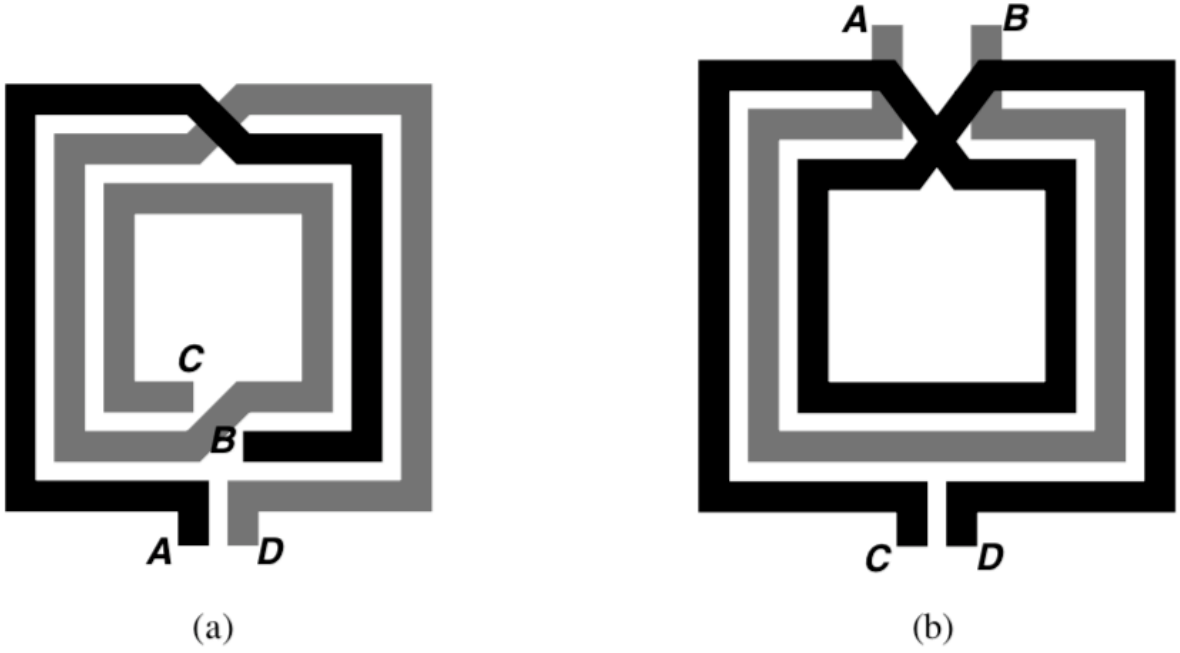


Figure 7.51 *One-to-two transformers (a) derived from a symmetric inductor, (b) formed as two symmetric inductors.*

Transformer Structures: examples - III

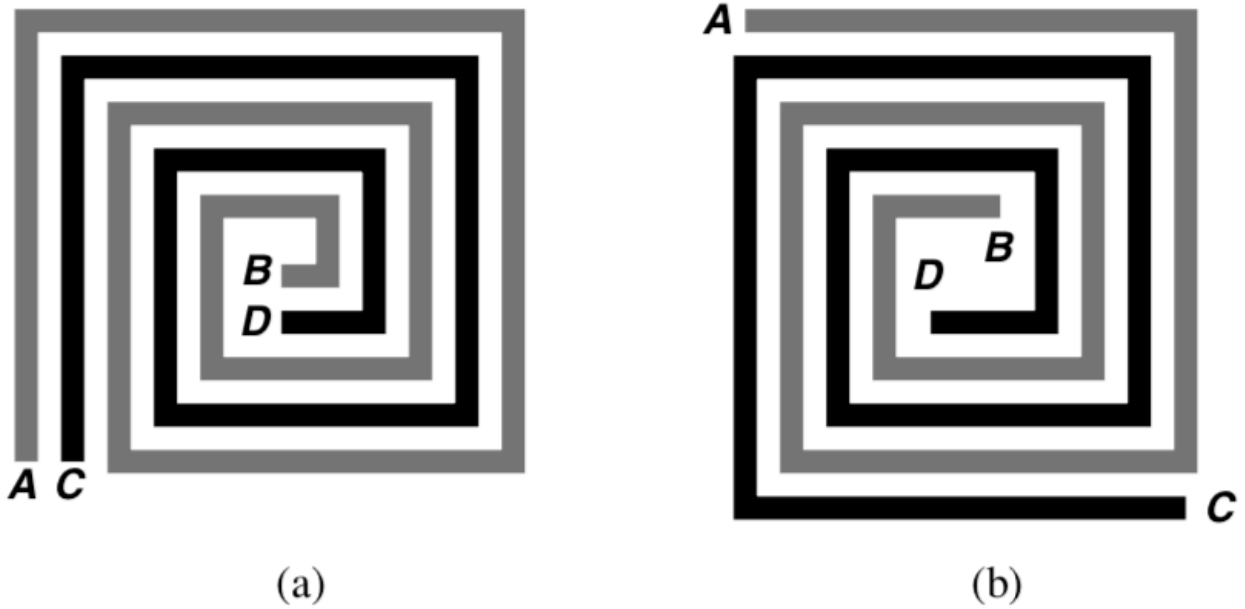
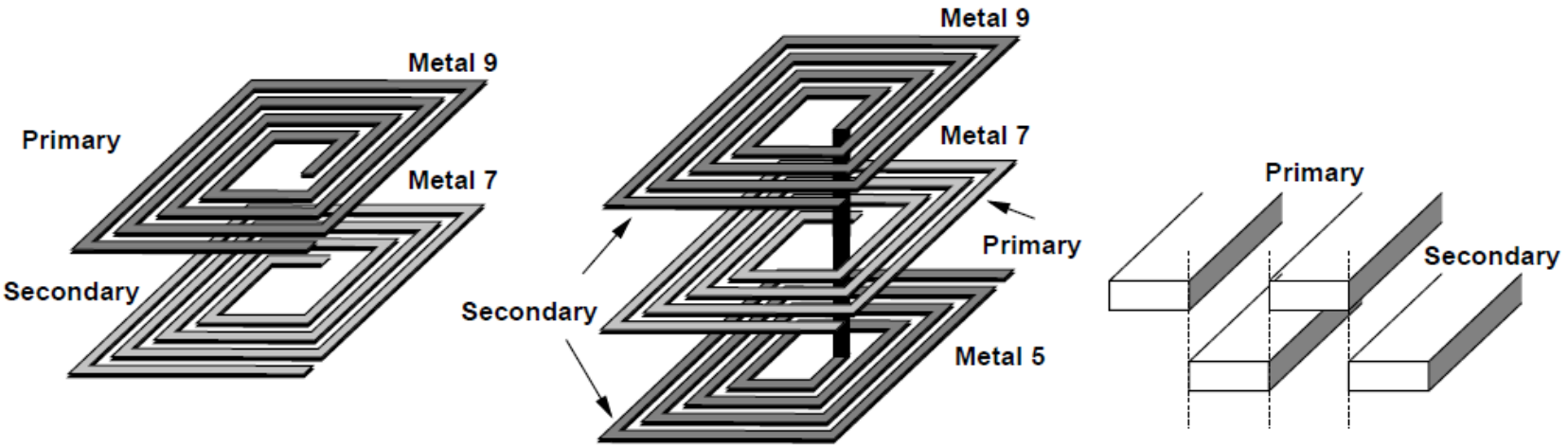


Figure 7.52 *(a) Transformer formed as two wires wound together, (b) alternative version with equal primary and secondary lengths.*

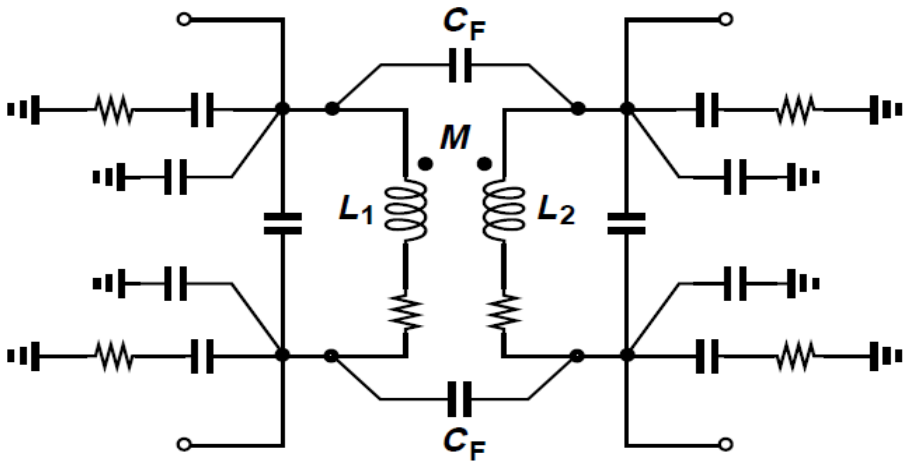
Stacked transformers

- Higher magnetic coupling.
- Unlike planar structures, primary and secondary can be identical and symmetrical.
- Overall area is less than planar structure.
- Larger capacitive coupling compared to planar structure.



Transformer modeling

- Due to high complexity of models, it is very difficult to find the values of each component from measurement or field simulations.
- Typically n-port with s-parameter tables in the simulators.
- Sometimes convergence difficulties, especially when f -> 0.



7.4 Transmission lines

- When the distance of a connection (wire) is comparable to the wavelength.
- f = 1 GHz => l = 30 cm, f = 100 GHz => 3 mm
- More PCB-level aspect + cables, unless very high frequency circuit.

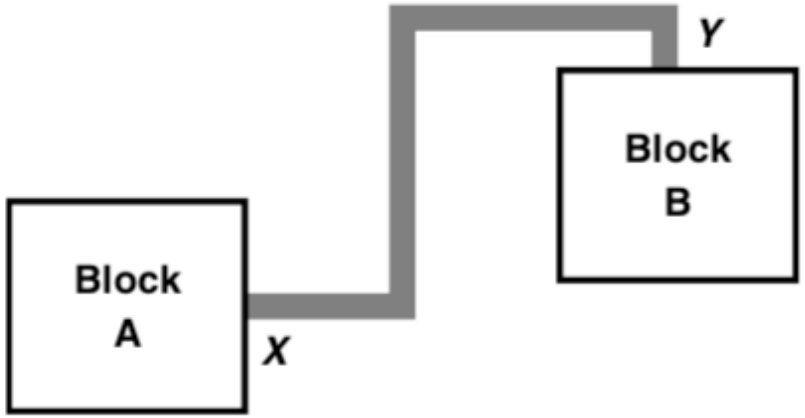


Figure 7.55 *Two circuit blocks connected by a long wire.*

Example 7.28

For the wire shown in Fig. 7.55, we also say the current "return path" is poorly-defined. Explain this attribute and its consequences.

Solution:

In the ideal situation, the signal current flowing through the wire from block *A* to block *B* returns through a ground plane [Fig. 7.56(a)]. In reality, however, due to the wire parasitics and the nonideal ground connection between the two blocks, some of the signal current flows through the substrate [Fig. 7.56(b)]. The complexity of the return path makes it difficult to accurately predict the behavior of the wire at high frequencies. Also, the coupling to the substrate creates leakage of the signal to other parts of the chip.

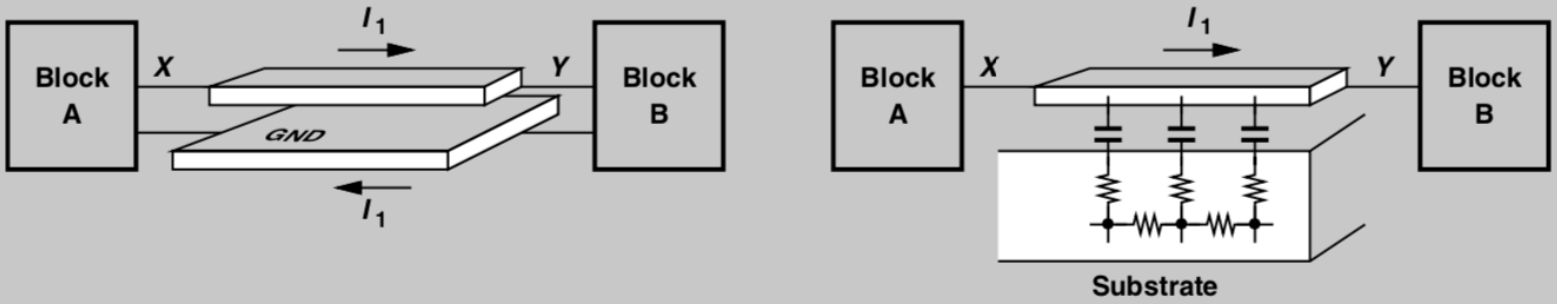
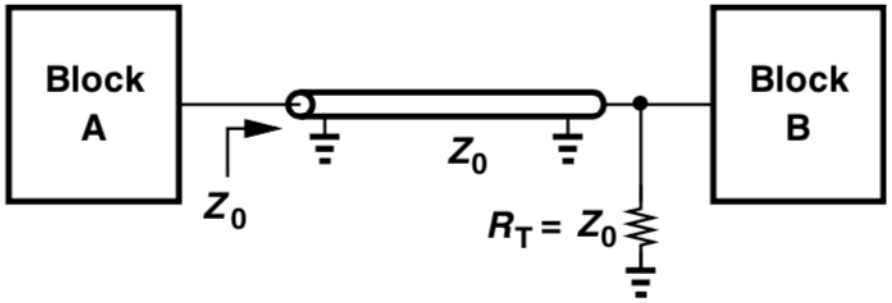
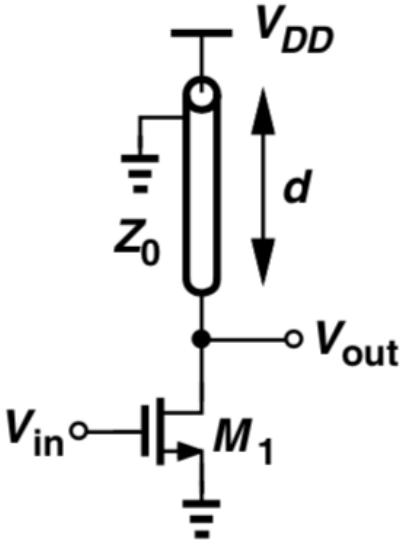


Figure 7.56 *(a) Current return path through a ground plane, (b) poor definition of current return path.*

Transmission lines



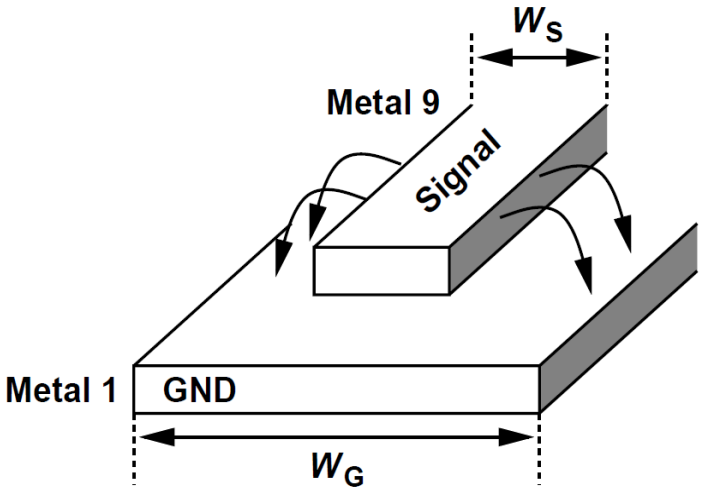
Connection between circuits blocks



Load inductor

Transmission lines

- Circuit + PCB: Microstrip lines realized in top-most metal layer and ground plane is in lower metal layer. Hence have minimum interaction between signal line and substrate.



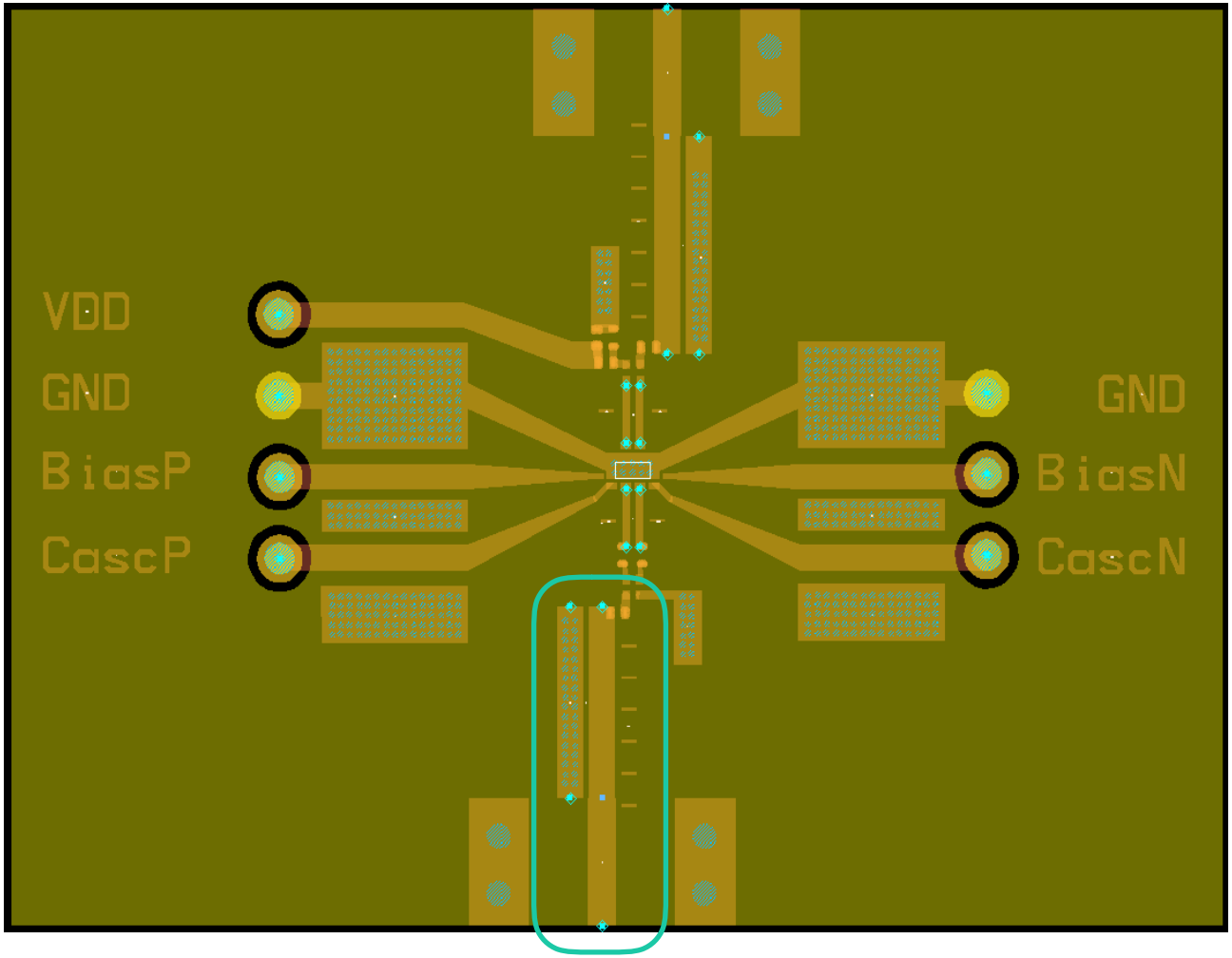
Transmission lines

- Characteristic impedance Z_0:

$$Z_{in}(d) = \frac{Z_L + jZ_0 \tan(\beta d)}{Z_0 + jZ_L \tan(\beta d)}$$

- d = length
- ß = 2*π/lambda
- E.g. if d= lambda/4 => $Z_{in} = Z_o^2/Z_L$ => impedance transformation (C -> L).

Transmission lines

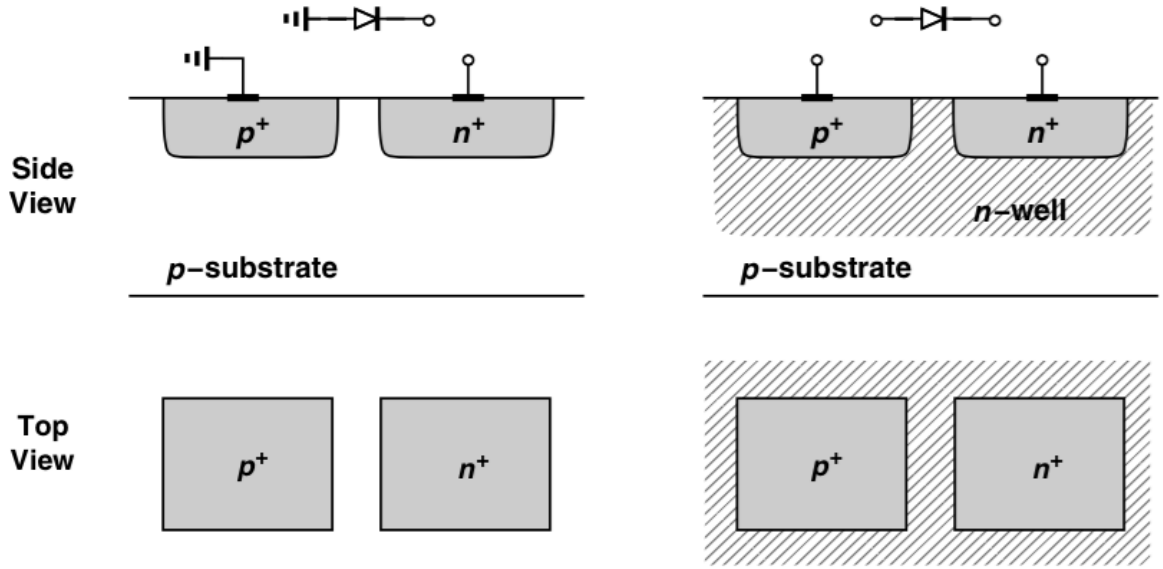


7.5 Varactors

- Varactor = voltage dependent capacitor
- Important properties:
  - capacitance range (vs. voltage)
  - quality factor (parasitic series resistance)
- Two ways to implement on an IC:
  - pn-junction (reverse-biased) - older technologies
  - MOSFET transistor - today

Varactors: pn-junction

- Reverse-biased pn-junction (diode)
- In most IC:s, the substrate is p- and grounded on the backside.



Varactors: pn-junction

- Geometry-dependent parasitics, hard to simulate and model.

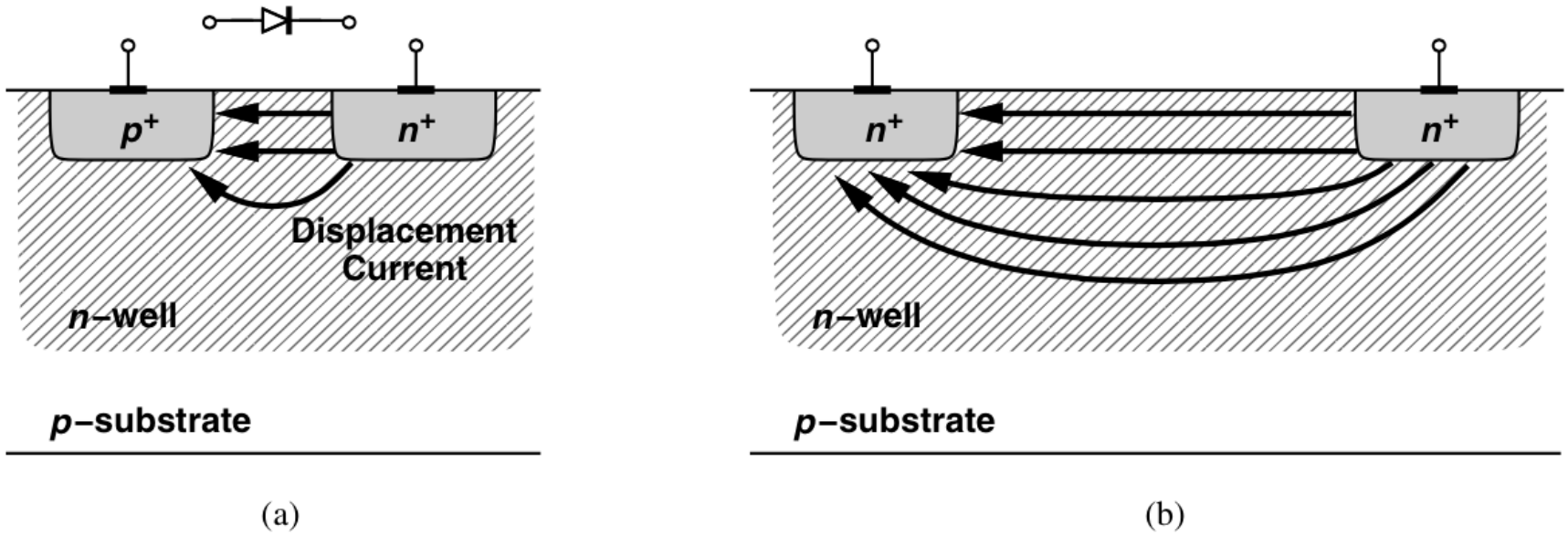
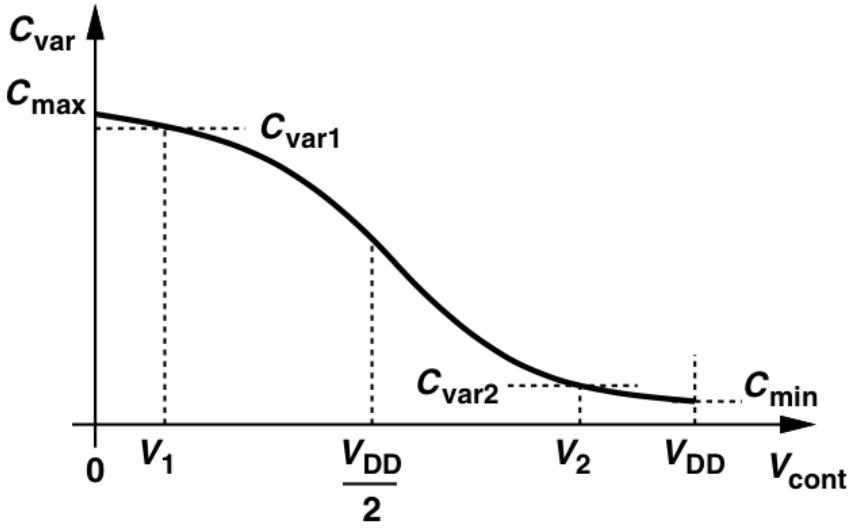


Figure 7.68 *Current distribution in a (a) varactor, (b) typical test structure.*

Varactors: pn-junction

- Capacitance for a planar reverse pn-junction at voltage V_D

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_D}{V_0}\right)^m},$$



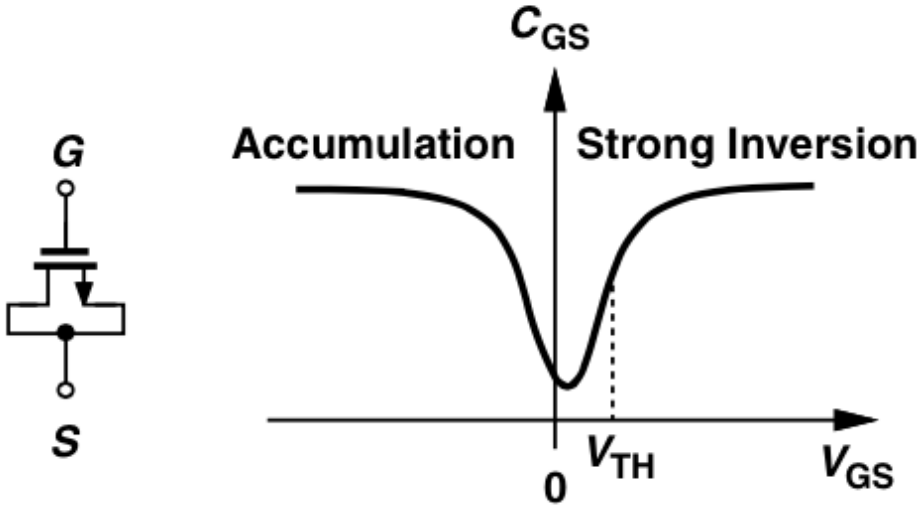
C_{j0} = cap at zero voltage

V_0 = "built-in potential" (about 0.7 V in silicon)

m ≈ 0.3 for CMOS

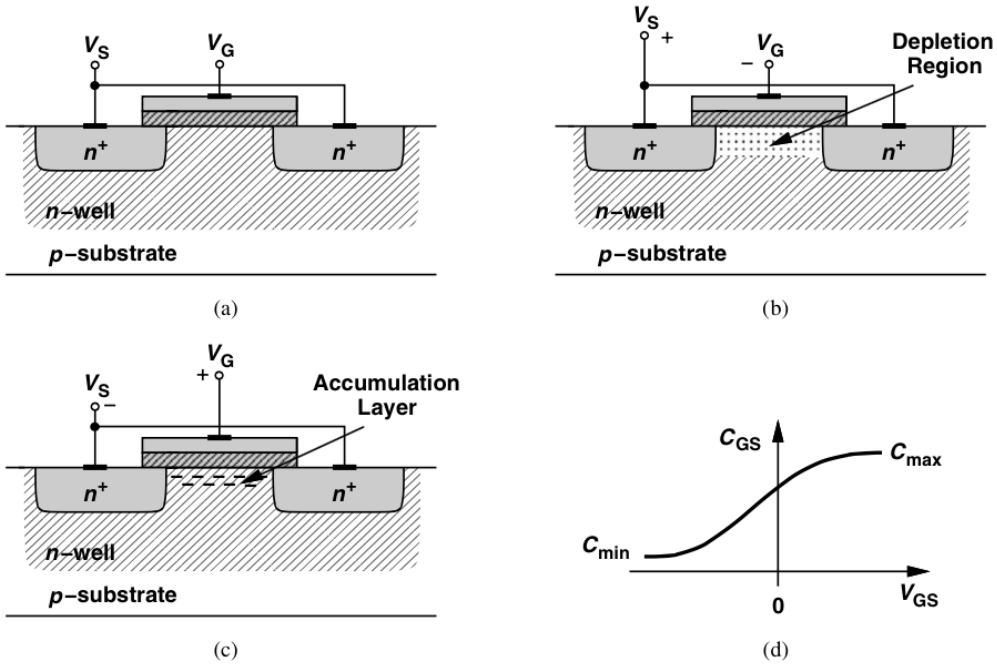
Varactors: MOSFET

- The gate-substrate capacitance of an ordinary MOSFET can also be used as a varactor.
- But characteristics of a normal transistor is not ideal for use as a C vs. V-device.



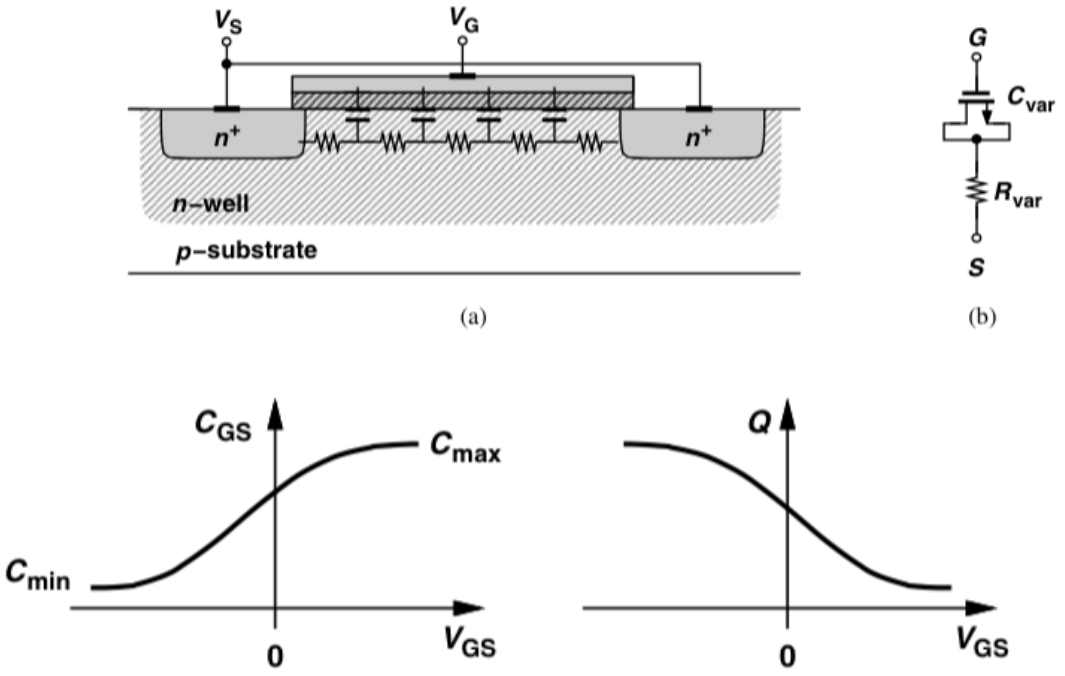
Varactors: MOSFET

- Instead, place the NMOS-transistor in an nwell. Now it does not work as a transistor anymore, just a capacitor with better characteristics. This is called an "accumulation-mode" MOS varactor.
- For 65 nm CMOS, C_{min} and C_{max} are reached at -/+ 0.5 V.



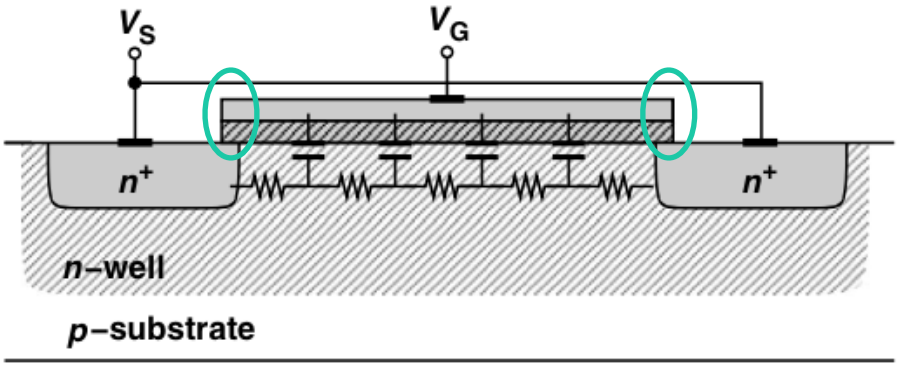
Varactors: MOSFET

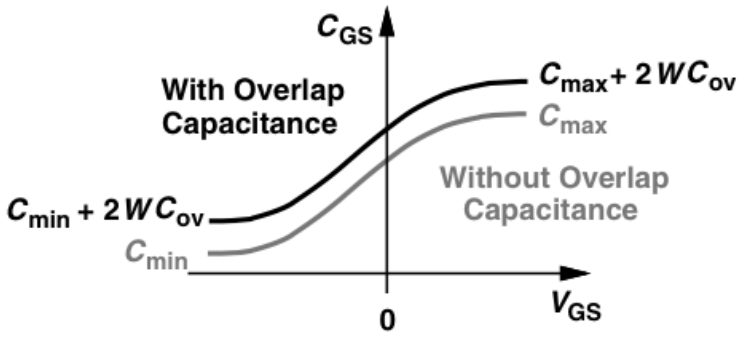
- The Q of MOS varactors is determined by the resistance between the source and drain terminals.
- Q also varies with C: Q = 1/(ωRC)

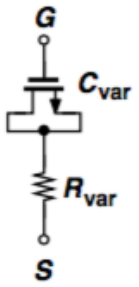


Varactors: MOSFET

- Overlap capacitance shifts the C/V characteristic up, yielding a ratio of $(C_{max} + 2W_{Cov})/(C_{min} + 2W_{Cov})$







- Typical C_{max}/C_{min} ratios = 2-4

Example 7.34

- A MOS varactor realized in 65-nm technology has an effective length of 50 nm and a C_{ov} of 0.09 fF/μm. If C_{ox} = 17 fF/μm^2, determine the largest capacitance range that the varactor can provide.

Assuming a width of 1 μm for the device, we have $2WC_{ov} = 0.18$ fF and a gate oxide capacitance of $17\,\text{fF}/\mu\text{m}^2 \times 1\,\mu\text{m} \times 50\,\text{nm} = 0.85$ fF. Thus, the minimum capacitance is 0.18 fF (if the series combination of the oxide and depletion capacitances is neglected), and the maximum capacitance reaches 0.85 fF + 0.18 fF = 1.03 fF. The largest possible capacitance ratio is therefore equal to 5.72. In practice, the series combination of the oxide and depletion capacitances is comparable to $2WC_{ov}$, reducing this ratio to about 2.5.

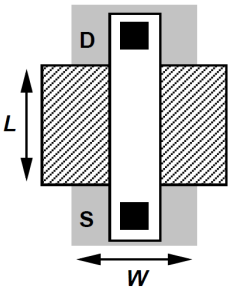
7.6 Constant capacitors

- Critical parameters of capacitors used in RF IC design:
  - Capacitance density
  - Parasitic capacitance
  - Q of the capacitor
- MOS capacitor
- MIM capacitor
- Metal plate (MOM) capacitor
- Fringe (grid) capacitor

MOS capacitor

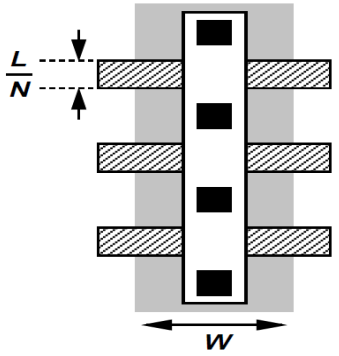
- One long finger having channel resistance

$$R_{on,a} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$



- Multiple short fingers having resistance

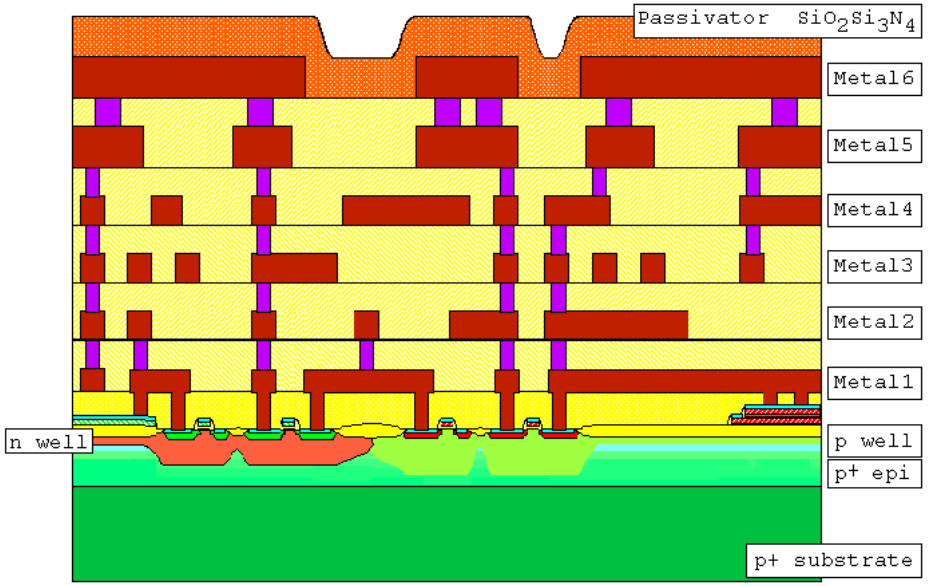
$$R_{on,u} = \frac{1}{\mu_n C_{ox} \frac{W}{L/N}(V_{GS} - V_{TH})}$$

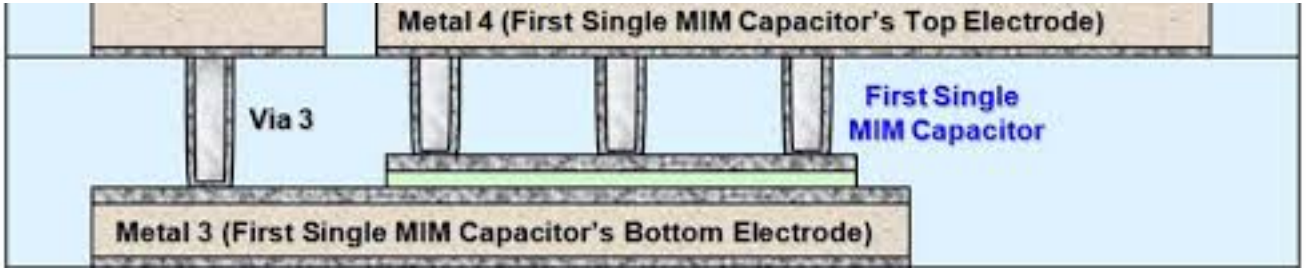


- Since N fingers appear in parallel, $R_{on,b} = R_{on,u}/N = R_{on,a}/N^2$. That is, the decomposition of the device into N parallel fingers reduces the resistance by a factor of N^2.

Metal-Insulator-Metal (MIM) Capacitor

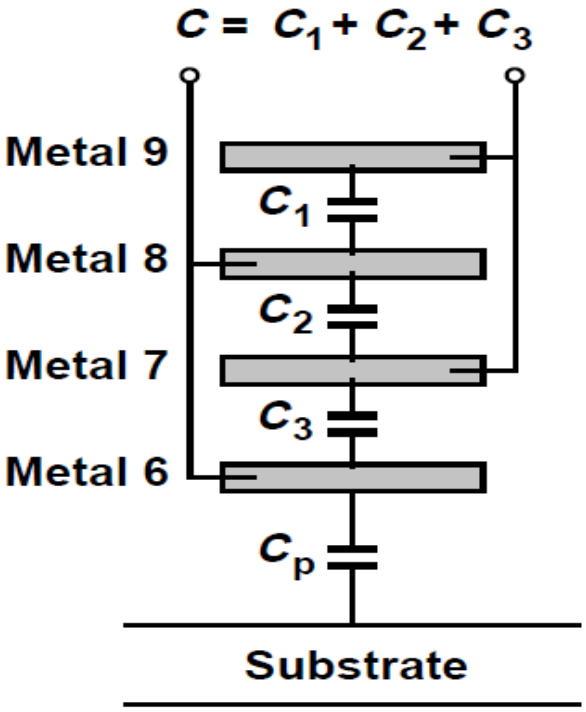
- Parallel plate capacitor.
- Usually 1-2 additional masks => thinner insulator to have better Cox/area.

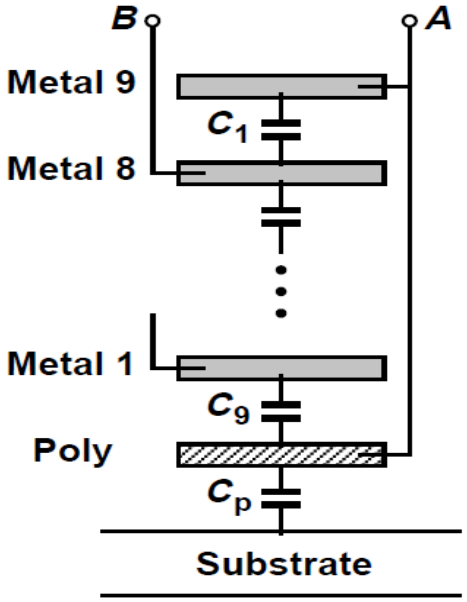


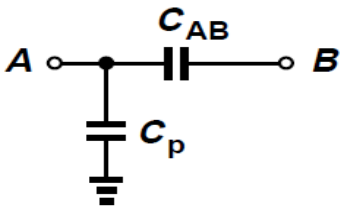


Metal-Plate (MOM) Capacitor

- Parallel plate capacitor.
- This structure employs planes in different metal layers







Fringe Capacitor

- Fringe capacitor consists of narrow metal lines with minimum spacing.
- The lateral electric field between adjacent metal lines leads to a high capacitance density.
- No additional masks or processing.