

Application-Specific Integrated Circuits

Programme course

6 credits

Applikationsspecifika integrerade kretsar

TSTE87

Valid from: 2018 Spring semester

Determined by Board of Studies for Electrical Engineering, Physics and Mathematics

Date determined 2017-01-25

Main field of study

Computer Science and Engineering, Electrical Engineering

Course level

Second cycle

Advancement level

A1X

Course offered for

- Computer Science and Engineering, M Sc in Engineering
- Electronics Design Engineering, M Sc in Engineering
- Applied Physics and Electrical Engineering, M Sc in Engineering
- Electronics Engineering, Master's programme
- Information Technology, M Sc in Engineering
- Applied Physics and Electrical Engineering International, M Sc in Engineering

Entry requirements

Note: Admission requirements for non-programme students usually also include admission requirements for the programme and threshold requirements for progression within the programme, or corresponding.

Prerequisites

Basic courses in digital circuits



Intended learning outcomes

General methods and principles used for designing and implementing application specific integrated circuits are presented. The emphasis is put on a systematic design methodology going from system specification down to complete integrated circuit. After completing the course you are expected to be able to:

- Analyze computational properties of signal processing algorithms
- Determine resource requirements for implementation of signal processing algorithms
- Determine the suitability of different types of architectures for implementation of signal processing algorithms
- Synthesize nearly optimal architectures
- Realize and evaluate different types of processing elements

As parts of the course the student is expected to be able to:

- Determine limits on the obtainable data rate
- Determine a computational order of operations
- Compute the latency and execution time of operations and determine the impact of these properties
- Determine computational graphs and optimize schedules
- Define and analyze different types of optimality in parts of the design flow
- Determine and optimize resource allocation and resource assignment
- Synthesize and analyze different architectures for signal processing systems
- Realize different types of processing elements using different arithemtic styles

Course content

System design and implementation using VLSI-technology or FPGA-technology of some signal processing applications, e.g., digital filters, FFT, and DCT. System specification, system architecture, analysis of computing properties of DSP algorithms. Synthesis of optimal DSP architectures. Conventional implementation methodologies. Processing elements and arithmetic. Implementation aspects.

Teaching and working methods

The course consists of lectures, exercises, computer and laboratory exercises.

Examination

LAB1	Laboratory Work	1.5 credits	U, G
TEN1	Written Examination	4.5 credits	U, 3, 4, 5

Grades

Four-grade scale, LiU, U, 3, 4, 5



Department

Institutionen för systemteknik

Director of Studies or equivalent

Tomas Svensson

Examiner

Oscar Gustafsson

Course website and other links

http://www.isy.liu.se/en/edu/kurs/TSTE87/

Education components

Preliminary scheduled hours: 68 h Recommended self-study hours: 92 h

Course literature

Wanhammar, L: DSP Integrated Circuits, Academic Press, 1999. ISBN 0127345302.



Common rules

Regulations (apply to LiU in its entirety)

The university is a government agency whose operations are regulated by legislation and ordinances, which include the Higher Education Act and the Higher Education Ordinance. In addition to legislation and ordinances, operations are subject to several policy documents. The Linköping University rule book collects currently valid decisions of a regulatory nature taken by the university board, the vice-chancellor and faculty/department boards.

LiU's rule book for education at first-cycle and second-cycle levels is available at http://styrdokument.liu.se/Regelsamling/Innehall/Utbildning_pa_grund-_och_avancerad_niva.

